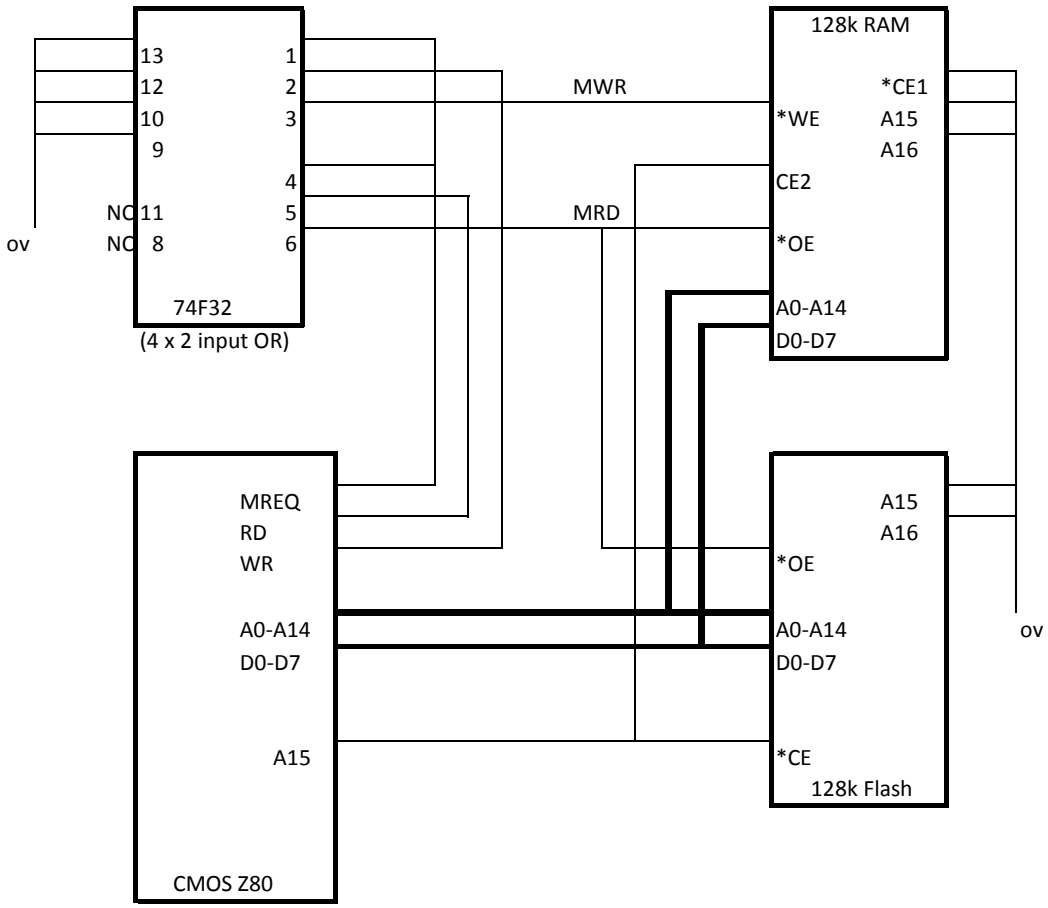

Simnple Z80 CPU Board
32k ROM, 32k RAM, achieved without any decode logic for maximum possible access speed
128k ran chip used as it has 2 chip selects, active low CE1 is tied to 0v, as are A15 and A16
active high CE2 connected to A15 ram is the active for upper 32k
128k Flash used for the ROM, active low CE connected to A15 rom is active for lower 32k
A15 and A16 of the ROM also tied low

74F32 high speed quadruple 2 input OR gate used to combine MREQ with the read and write signals from the Z80 to create memory read and write signals for the ROM and RAM

On the test Baord D0-D7, A0-A7 and the Z80 control signals are connected to the backplane connector to allow access to the V9958 Video board.

27Mhz clock curcuit is the same style as the 4mhz clock in the MTX manual.
It uses 2, 470R resistors, 2 gates from a 74F04 and a 10nf ceramic capacitor